WHAT IS CLAIMED IS:

1. A semiconductor device, comprising: plural electrode pads arranged within active regions of a main surface of a semiconductor chip; and plural wiring layers arranged over the main surface of said semiconductor chip,

wherein in at least one wiring layer selected among said plural wiring layers and arranged below the plural electrode pads, occupation rates of wirings arranged in the respective planar regions of the plural electrode pads become uniform.

2. A semiconductor device, comprising: plural electrode pads arranged within active regions of a main surface of a semiconductor chip; and plural wiring layers arranged over the main surface of said semiconductor chip,

wherein in each wiring layer of the plural wiring layers and arranged below the plural electrode pads, occupation rates of wirings arranged in the respective planar regions of the plural electrode pads become uniform.

3. A semiconductor device according to Claim 1,

wherein the occupation rates of wirings arranged within the planar regions of said plural electrode pads

are, respectively, at 50% or over.

4. A semiconductor device according to Claim 1, wherein variations in the occupation rates of wirings arranged within the planar regions of said plural electrode pads are, respectively, within 10%.

5. A semiconductor device according to Claim 1, wherein variations in the occupation rates of wirings arranged within the planar regions of said plural electrode pads are, respectively, within 5%.

6. A semiconductor device, comprising: plural electrode pads arranged within active regions of a main surface of a semiconductor chip; and plural wiring layers arranged over the main surface of said semiconductor chip, wherein in at least one wiring layer selected among the plural wiring layers and arranged below the plural electrode pads, variations in the occupation rates of wirings arranged within planar regions of said plural electrode pads are, respectively, within 10%.

7. A semiconductor device, comprising: plural electrode pads arranged within active regions of a main surface of a semiconductor chip; and plural wiring layers arranged

over the main surface of said semiconductor chip,

wherein in at least one wiring layer selected among the plural wiring layers and arranged below the plural electrode pads, occupation rates of wirings arranged within planar regions of said plural electrode pads are, respectively, 50% or over.

8. A semiconductor device according to Claim 1, wherein said plural electrode pads include plural dummy electrode pads and at least one of the plural dummy electrode pads has an area larger than an electrode pad for integrated circuit taken from said plural electrode pads.

9. A semiconductor device, comprising: plural electrode pads arranged within active regions of a main surface of a semiconductor chip; and plural wiring layers arranged over the main surface of said semiconductor chip,

wherein said plural electrode pads include an electrode pad for integrated circuit formed in the main surface of said semiconductor chip and a dummy electrode pad, and the active regions are provided in the main surface of said semiconductor chip as an underlying layer of said electrode pads for integrated circuit and said dummy electrode pads.

10. A semiconductor device according to Claim 9, wherein said active region below said dummy electrode pad is provided as a dummy active region.

11. A semiconductor device according to Claim 1, wherein a bump electrode is bonded to said plural electrode pads, respectively.

12. A semiconductor device according to Claim 1, wherein a dummy wiring, which is irrelevant to elements and wirings of said semiconductor chip and is thus in a floating condition, is arranged within the planar regions of the plural electrode pads.

13. A semiconductor device according to Claim 1, wherein a wiring-removed portion is formed at part of the wirings arranged within the planar regions of said plural electrode pads.

14. A semiconductor device according to Claim 1, wherein a circuit for driving a liquid crystal display is formed in the main surface of said semiconductor chip.

15. A semiconductor device according to Claim 1, wherein a semiconductor element is formed in the semiconductor

chip within said active regions.

16. A method for manufacturing a semiconductor device, comprising the steps of:

(a) forming an isolation portion and an active region in a main surface of a semiconductor substrate;

(b) forming plural wiring layers over the main surface of said semiconductor substrate; and

(c) forming an insulating film to cover the uppermost wiring of said plural wiring layers therewith, and subsequently forming openings in the insulating film within the active region so that part of said uppermost wiring layer is exposed, thereby forming plural electrode pads,

wherein in at least one wiring layer of said plural wiring layers below said plural electrode pads, wirings are formed such that occupation rates of the wirings within planar regions of said plural electrode pads are made uniform.

17. A method for manufacturing a semiconductor device, comprising the steps of:

(a) forming an isolation portion and an active region in a main surface of a semiconductor substrate;

(b) forming plural wiring layers over the main surface

of said semiconductor substrate; and

(c) forming an insulating film to cover the uppermost wiring of said plural wiring layers therewith, and subsequently forming openings in the insulating film within the active region so that part of said uppermost wiring layer is exposed, thereby forming plural electrode pads,

wherein in each of said plural wiring layers below said plural electrode pads, wirings are formed such that occupation rates of the wirings within planar regions of said plural electrode pads are made uniform.

18. A method according to Claim 16, wherein occupation rates of the wirings arranged within the planar regions of said plural electrode pads are, respectively, 50% or over.

19. A method according to Claim 16, wherein variations in occupation rate of wirings arranged within the planar regions of said plural electrode pads are, respectively, within 10%.

20. A method according to Claim 16, wherein variations in occupation rate of the wirings arranged within the planar regions of said plural electrode pads are,

respectively, within 5%.

21. A method for manufacturing a semiconductor device, comprising the steps of:

(a) forming an isolation portion and an active region in a main surface of a semiconductor substrate;

(b) forming plural wiring layers over the main surface of said semiconductor substrate; and

(c) forming an insulating film to cover the uppermost wiring of said plural wiring layers therewith, and subsequently forming openings in the insulating film within the active region so that part of said uppermost wiring layer is exposed, thereby forming plural electrode pads,

wherein in at least one wiring layer of said plural wiring layers below said plural electrode pads, variations in occupation rate of the wirings within planar regions of said plural electrode pads are within 10%, respectively.

22. A method for manufacturing a semiconductor device, comprising the steps of:

(a) forming an isolation portion and an active region in a main surface of a semiconductor substrate;

(b) forming plural wiring layers over the main surface

of said semiconductor substrate; and

(c) forming an insulating film to cover the uppermost wiring of said plural wiring layers therewith, and subsequently forming openings in the insulating film within the active region so that part of said uppermost wiring layer is exposed, thereby forming plural electrode pads,

wherein in at least one wiring layer of said plural wiring layers below said plural electrode pads, occupation rates of the wirings within planar regions of said plural electrode pads are 50% or over, respectively.

23. A method for manufacturing a semiconductor device, comprising the steps of:

(a) forming an isolation portion and an active region in a main surface of a semiconductor substrate;

(b) forming plural wiring layers over the main surface of said semiconductor substrate; and

(c) forming an insulating film to cover the uppermost wiring of said plural wiring layers therewith, and subsequently forming openings in the insulating film within the active region so that part of said uppermost wiring layer is exposed, thereby forming plural electrode pads,

wherein said plural electrode pads include an

electrode pad for integrated circuit form on the main surface of said semiconductor substrate and a dummy electrode pad, and said active region is formed in the main surface of said semiconductor substrate as an underlying layer for said electrode pad for integrated circuit and said dummy pad, respectively.

24. A method according to Claim 23, wherein said active region serving as an underlying layer for said dummy electrode pad is a dummy active region.

25. A method according to Claim 16, further comprising, after the step (c), a step of bonding bump electrodes to said plural electrode pads.

26. A method according to Claim 25, further comprising a step of subjecting the bump electrodes of said plural electrode pads and wirings of a glass substrate to pressure bonding in block.

27. A method according to Claim 25, further comprising a step of subjecting said plural electrode pads and leads of a tape to pressure bonding via said bump electrodes in block.

28. A method according to Claim 16, wherein a dummy wiring is formed within the planar regions of said plural electrode pads.

29. A method according to Claim 16, wherein a wiring-removed portion is formed at part of wirings arranged within planar regions of the plural electrode pads.

30. A method according to Claim 30, wherein underlying layers for wiring layers of said plural wiring layers where said plural electrode pads are arranged are polished by a chemical mechanical polishing method.

31. A method according to Claim 16, wherein a circuit for driving a liquid crystal display is formed in the main surface of said semiconductor substrate.

32. A method according to Claim 16, wherein a semiconductor element is formed in said active region.

33. A method for manufacturing a semiconductor device, comprising the steps of:

(a) providing a semiconductor chip which includes: plural electrode pads arranged within active regions of

a main surface of a semiconductor substrate; plural wiring layers arranged over the main surface of said semiconductor substrate and provided below the plural electrode pads; and a bump electrode for each of said plural electrode pads, in which in at least one wiring layer of the plural wiring layers, occupation rates of wirings arranged within the respective planar regions of said plural electrode pads are made uniform; and

(b) subjecting the bump electrodes of said plural electrode pads and the wirings of a glass substrate to pressure bonding.

34. A method according to Claim 33, wherein the bump electrodes of said plural electrode pads and the wirings of the glass substrate are pressure-bonded in block in such a state that an anisotropic conductive film is interposed between a plural electrode pad-forming surface of said semiconductor substrate and a wiring-forming surface of said glass substrate.

35. A method according to Claim 33, wherein said glass substrate has a liquid panel mounted thereon.

36. The semiconductor device according to Claim 2, wherein occupation rates of wirings arranged within the

respective planar regions of said plural electrode pads are 50% or over.

37. The semiconductor device according to Claim 2, wherein said plural electrode pads include plural dummy pads, at least one of which has an area larger than an electrode pad for integrated circuit taken from said plural electrode pads.

38. The semiconductor device according to Claim 37, wherein the active regions below the dummy electrode pads are dummy active regions, respectively.

39. The semiconductor device according to Claim 2, wherein a dummy wiring, which is irrelevant to elements and wirings of said semiconductor chip and is thus in a floating condition, is arranged within the planar regions of the plural electrode pads.

40. The semiconductor device according to Claim 2, wherein a wiring-removed portion is formed at part of the wirings arranged within the planar regions of said plural electrode pads.